REMARKS

In accordance with the foregoing, the specification and claims 1-12 and 14-16 have been amended and claim 13 has been canceled, without prejudice or disclaimer.

Claims 1-12 and 14-16 are pending and under consideration.

OBJECTIONS TO THE DRAWINGS:

In the Office Action, at page 2, the drawings were objected to. In view of the accompanying REPLACEMENT DRAWINGS of FIGS. 1-3, it is respectfully requested that the drawings be reconsidered and that the rejection to the drawings be withdrawn.

REJECTION UNDER 35 U.S.C. § 102:

In the Office Action, at page 2, claims 1, 2, 4, 6, 7, 10-12, and 16 were rejected under 35 U.S.C. § 102 in view of U.S. Patent No. 6, 226,756 to Mueller ("Mueller"). This rejection is traversed and reconsideration is requested.

FIG. 3 of Mueller is a schematic block diagram illustration of an interface 104 (FIG. 1) coupled with configuration inputs 106 and mounted on interface card 200 in FIG. 2. An interface 104a includes an emulator 305 and a processor 310. The emulator 305 includes a clock generator 330, a reset circuit 315, a configuration logic circuit 320 and a clock duplicator and buffer circuit 325. A "hard" reset is provided to initialize the system logic and processor in computer system 100 to a predetermined state. See column 7, lines 49-63 of Mueller. For example, system hardware is reset to default values and system logic is set to appropriate initial values--memory size, system device recognition and other system default values. In the embodiment of FIG. 3, reset circuit 315 of the emulator 305 provides signal 335 to system logic 108 to indicate a hard reset. See column 7, lines 63-67, and column 8, lines 1-3 of Mueller.

Accordingly, in Mueller, the reset signal is generated when the emulator 305 receives an external reset signal. However, rather than teaching or suggesting, "a system reset output section generating and outputting a system reset signal on the basis of an external reset signal . . wherein said system reset signal output from said system reset output section is supplied to both chips of said central processing section and said peripheral control section," as recited in independent claim 1, Mueller provides the reset signal from the emulator 305 for the processor 310 and the system logic 108.

Assuming, arguendo, that the push-button result is interpreted as the external reset

signal, there is nothing in Mueller that teaches or suggests that based on the push-button reset a system reset signal output "is supplied to both chips of said central processing section and said peripheral control section," as recited in independent claim 1. Instead, the reset signal from the emulator 305 is supplied to the processor 310 and the system logic 108.

One of the many advantages of the system reset output section of the present invention is that the system reset signal may be distributed and supplied to separate chips (e.g., a processor and a companion chip) on a basis of the emulator reset signal and the external reset signal. Accordingly, it is respectfully asserted that Mueller fails to teach or suggest all the claimed features of independent claim 1. It is respectfully requested that independent claim 1 and related dependent claims be allowed.

Referring to independent claim 10, this claim recites, "a reset selection section selectively outputting, as a system reset signal, one of an external reset signal and an emulator reset signal based on a reset instruction from an emulator for independently implementing a function of said central processing section, wherein said system reset signal output from said reset selection section is supplied to both chips of said central processing section and said peripheral control section." Because independent claim 10 includes similar claim features as those recited in independent claim 1, although of different scope, the arguments presented above supporting the patentability of independent claim 1 are incorporated herein to support the patentability of independent claim 10.

Furthermore, the Office Action refers to column 7, lines 49-67, and column 8, lines 1-3, as providing "a reset selection section selectively outputting, as a system reset signal, one of an external reset signal and an emulator reset signal based on a reset instruction from an emulator for independently implementing a function of said central processing section," as recited in independent claim 10. Applicants respectfully traverse such assertion. Mueller provides a "hard" reset from the emulator in the interface 104a to the system logic and processor and the reset circuit 315 provides signal 355 to system logic 108 to indicate a hard reset. However, nothing in Mueller teaches or suggests that the reset generation selectively outputs "as a system reset signal, one of an external reset signal and an emulator reset signal based on a reset instruction from an emulator," as recited in independent claim 10. Accordingly, it is respectfully asserted that Mueller fails to teach or suggest all the claimed features of independent claim 10. It is respectfully requested that independent claim 10 and related dependent claims be allowed.

Independent claim 16 recites, "selectively outputting, as a system reset signal, one of an

external reset signal and an emulator reset signal based on a reset instruction from an emulator for independently implementing a function of said central processing section; and supplying said system reset signal to both chips of said central processing section and said peripheral control section." Because independent claim 16 includes similar claim features as those recited in independent claims 1 and 10, although of different scope, the arguments presented above supporting the patentability of independent claims 1 and 10 are incorporated herein to support the patentability of independent claim 16. It is respectfully requested that independent claim 16 be allowed.

In the Office Action, at page 6, claim 13 was rejected under 35 U.S.C. § 102 in view of U.S. Patent No. 6, 415,393 to Satoh ("Satoh"). This rejection is traversed and reconsideration is requested.

Because independent claim 13 has been cancelled, it is respectfully asserted that the rejection to the claim is rendered moot.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at page 6, claim 3 was rejected under 35 U.S.C. § 103 in view of Mueller. The reasons for the rejection are set forth in the Office Action and therefore not repeated. The rejection is traversed and reconsideration is requested.

Because dependent claim 3 depends from independent claim 1, Mueller must teach or suggest all the claimed features of independent claim 1. Accordingly, the arguments presented above supporting the patentability of independent claim 1 in view of Mueller are incorporated herein.

According to the Office Action, without providing any basis from a reference, it is conclusively asserted that "it would have been obvious to a person skilled in the art at the time the invention was made to put the system reset output section in the chip of the peripheral control section. It would have been obvious because Mueller discloses that his invention is intended to cover various equivalent arrangements within the scope." However, it is improper to merely deem something obvious without any teaching/suggestion from the cited reference, or the taking of Official Notice for the particular claimed feature for which it refers. If the U.S. Patent and Trademark Office wishes to take Official Notice that the proposed structural and functional modification is notoriously well known, it is respectfully requested that supporting evidence be provided. The Federal Circuit has cautioned that an Examiner must show reasons

that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. In re Rouffet, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998).

The outstanding Office Action has provided no explicit support of what the purported well-known features encompass or how the determination of those features as being well known has been determined. Rather, the Office Action only cites Mueller, without pointing how the claimed features have been determined as being well known.

Only the present invention sets forth all the claimed features, as well as the motivation for combining the same. The outstanding rejection would appear to have taken the teachings of the present invention such that a combination of "well known features" and Mueller, as set forth in the Office Action, would disclose the presently claimed invention. See W.L. Gore & Assocs. Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983). It is respectfully requested that independent claim 1 and related dependent claims be allowed.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at page 7, claims 5, 8, and 9 were rejected under 35 U.S.C. § 103 in view of Mueller and U.S. Patent No. 6, 415,393 to Satoh ("Satoh"). The reasons for the rejection are set forth in the Office Action and therefore not repeated. The rejection is traversed and reconsideration is requested.

Because dependent claims 5, 8, and 9 depend from independent claim 1, Mueller and Satoh, individually or combined, must teach or suggest all the claimed features of independent claim 1. Accordingly, the arguments presented above supporting the patentability of independent claim 1 in view of Mueller are incorporated herein.

Referring to Satoh, this reference generally describes an ICE system capable of debugging an integrated circuit device while it is in a development stage. See column 1, lines 14-20 of Satoh. A bus control unit switches a destination to be connected to a central processing unit from an external bus to the inspection control circuit in the inspection mode when the address of an access destination issued by the central processing unit agrees with the predetermined address. See column 3, lines 43-58 of Satoh. Further, a reset input signal entered from the external source is masked when an MTR bit is set to "1." See column 8, lines 47-61 of Satoh. When a CPU core 41 enters a debug mode, a reset input signal entered from

an external source is always masked irrespective of the MTR bit in order to carry out a monitoring process. See column 9, lines 36-48 of Satoh.

However, similarly to Mueller, Satoh is silent as to teaching or suggesting, "a system reset output section generating and outputting a system reset signal on the basis of an external reset signal and an emulator reset signal based on a reset instruction from the emulator to independently implement a function of said central processing section, wherein said system reset signal output from said system reset output section is supplied to both chips of said central processing section and said peripheral control section," as recited in independent claim 1. Nothing in Mueller and Satoh, individually or combined, teach or suggest that the reset signal is output "on the basis of an external reset signal" and that the emulator reset signal is output "based on a reset instruction from the emulator to independently implement a function of said central processing section," as recited in independent claim 1. Accordingly, it is respectfully asserted that Mueller and Satoh, individually or combined, fail to teach or suggest all the claimed features of independent claim 1. It is respectfully requested that independent claim 1 and related dependent claims be allowed

In the Office Action, at page 8, claims 14 and 15 were rejected under 35 U.S.C. § 103 in view of Mueller and Satoh. The reasons for the rejection are set forth in the Office Action and therefore not repeated. The rejection is traversed and reconsideration is requested.

The descriptions of Mueller and Satoh presented above are incorporated herein.

The Office Action correctly recognized that Mueller fails to teach or suggest, "masking an external reset signal when an emulator that independently implements a function of said central processing section is in operation," as recited in independent claim 14. However, on the second paragraph of page 9 of the Office Action, it is indicated that Mueller provides "generating an external reset signal or an emulator reset signal based on a reset instruction from the emulator." In view of the foregoing, it appears that some of the claimed features of independent claim 14 are being overlooked in the Office Action. If it is conceded that Mueller fails to teach or suggest "masking an external reset signal when an emulator that independently implements a function of said central processing section is in operation," as recited in independent claim 14, it also follows that Mueller fails to teach or suggest, "generating a system reset signal **on the basis of the masked external reset signal and an emulator reset signal** based on a reset instruction from said emulator," emphasis added, as recited in independent claim 14. Even assuming, arguendo, that Mueller provides generating the reset signal on the basis of the emulator reset signal, Mueller is silent as to generating the system reset signal on the basis of "the masked

external reset signal and an emulator reset signal based on a reset instruction from said emulator," as recited in independent claim 14.

According to Satoh, a reset input signal entered from the external source is masked when an MTR bit is set to "1." See column 8, lines 47-61 of Satoh. However, similarly to Mueller, Satoh is silent as to teaching or suggesting, "masking an external reset signal when an emulator that independently implements a function of said central processing section is in operation; generating a system reset signal on the basis of the masked external reset signal and an emulator reset signal based on a reset instruction from said emulator," as recited in independent claim 14. Nothing in Mueller and Satoh, individually or combined, teach or suggest that the masking is based on "the masked external reset signal and an emulator reset signal based on a reset instruction from said emulator," as recited in independent claim 14. Accordingly, it is respectfully asserted that Mueller and Satoh, individually or combined, fail to teach or suggest all the claimed features of independent claim 14. It is respectfully requested that independent claim 14 and related dependent claim 15 be allowed

Further, the motivation provided in the Office Action to combine the references is "because Satoh teaches an easily implemented protocol for handling an external reset when an emulator is in operation." However, nothing in either reference suggests or supports the purported combination of the references set forth in the Office Action. It is submitted that the reason why no such showing was made is because the prior art of record individually or combined, fail to teach, suggest, or otherwise provide the motivation needed to make such a modification. "To support the conclusion that the claimed combination is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed combination. It is to be noted that simplicity and hindsight are not proper criteria for resolving the issue of obviousness." Ex Parte Clapp, 227 USPQ 972, 973 (B.P.A.I. 1985).

Accordingly, in view of the foregoing, it is respectfully asserted that the prima facie obviousness rejection fails on its face and, accordingly, the combination of the references cited fails to teach or suggest a trading card comprising "a housing unit containing and protecting the data storage unit, wherein the housing unit comprises a serial number identifying the trading card," as recited in independent claim 14.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance, which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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